REMARKS

In view of the following remarks, Applicants respectfully request reconsideration and allowance of the subject application. This amendment is believed to be fully responsive to all issues raised in the July 20, 2004, Office action ("Office action").

Objections to the Claims

The Examiner has objected to claim 7, which was canceled in the Applicant's previous response. Claim 7, having been previously canceled, is no longer under examination. The Office Action itself indicates in the Office Action Summary that "Claim(s) 1 – 6, 15 – 20, 22 – 26 and 28 – 44 is/are pending in the application." Because claim 7 is no longer pending in the Application, the objection is improper.

Nevertheless, in support of the objection, the Examiner asserts that "additional fees for claim 7, previously examined but now cancelled, have not been received."

The Examiner's request for additional fees is contrary to the rules set forth in the Manual of Patent Examining Procedure (MPEP).

> "The initial determination, for fee purposes, as to whether a claim is dependent must be made by persons other than examiners; it is necessary, at that time, to accept as dependent virtually every claim which refers to another claim, without determining whether there is actually a true dependent relationship. The initial acceptance of a claim as a dependent claim does not, however, preclude a subsequent holding by the examiner that a claim is not a proper dependent claim. Any claim which is in dependent form but which is so worded that it, in fact is not, as, for example, it does not include

every limitation of the claim on which it depends, will be required to be *canceled* as not being a proper dependent claim..." MPEP § 608.01(n) II (emphasis added).

The MPEP clearly precludes the Examiner from making the determination, for fee purposes, as to whether a claim is dependent. If the Examiner believes that claim 7, prior to its cancellation, was actually an independent claim, the Examiner's only recourse was to object to the claim as not being in proper dependent form.

Applicants respectfully disagree with the Examiner's assertion that claim 7, when initially filed, was an independent claim. In any event, the Examiner cannot properly make the determination as to whether claim 7 was dependent or independent for fee purposes. Furthermore, the Examiner cannot now properly object to claim 7 because claim 7 is not pending.

As such, Applicants respectfully request that the objection to claim 7 be withdrawn.

CLAIM REJECTIONS

Claims Rejected Under - 35 USC §102(b)

Each of claims 1-6, 15-20, 22-26 and 28-44 has been rejected under 35 USC §102(b) as being anticipated by Bruce et al. (USPN 6,000,006). Additionally, each of claims 1-6, 15-20, 22-26 and 28-44 has been rejected under 35 USC §102(b) as being anticipated by either one of Mitani (USPN 6,663,986) or Fujimoto et al. (USPN 6,377,500). Bruce et al., Mitani, and Fujimoto et al. together are referred to

hereinafter collectively as the "cited references". Applicants traverse these rejections.

Discussion of Rejection

Improper Choice Of Prior Art

It is Applicants' position that the Examiner has improperly rejected the claims with multiple, merely cumulative references. As noted in the Manual of Patent Examining Procedure (MPEP), the Examiner should use only the single most pertinent reference in a 35 U.S.C. 102 rejection.

> "Normally, only one reference should be used in making a rejection under 35 U.S.C. 102." See MPEP 2131.01 (emphasis added).

> "CHOICE OF PRIOR ART; BEST AVAILABLE
> Prior art rejections should ordinarily be confined strictly to the best available art...." See MPEP § 706.02 I (emphasis added).

In the Office Action, three references were applied to all the pending claims:

> "4. Claims 1-6, 15-20, 22-26 and 28-44 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bruce et al., U.S. 6,000,006...
> 5. Claims 1-6, 15-20, 22-26 and 28-44 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Mitani, U.S. 6,633,956...
> 6. Claims 1-6, 15-20, 22-26 and 28-44 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Fujimoto et al., U.S. 6,377,500."

The multiple rejections based on Bruce, Mitani, and Fujimoto are merely cumulative. The multiple references are not provided for purposes of enablement of the references, to explain the meaning of a term in a reference, to show

inherency, or for any other reason that is allowed by the MPEP. Each of the multiple rejections merely rejects the claims as being anticipated by a different reference. It is entirely unclear which reference the Examiner deems the best available.

As such, the Applicants have been given the burden of having to overcome multiple 35 U.S.C. 102 rejections under multiple references for each claim. Placing such a burden of the Applicants is clearly contrary to well established PTO practice and the MPEP. Applicants request that if the Office maintains the rejections of all claims under 35 U.S.C 102, that the Office select the single, best reference in accordance with the MPEP.

Prima facie case of non-patentability not met

It is Applicants' position that the reasoning set forth in the Office action for rejecting claims 1-6, 15-20, 22-26 and 28-44 are so minimal and unspecific with respect to the claims and the cited references that the Office has failed meet its burden of presenting at least a prima facie case of non-patentability. More particularly, the Office has failed to meet its burden of proving anticipation.

As stated by the Court of Appeals for the Federal Circuit, "Under section 102(b), anticipation requires that the prior art reference disclose, either expressly or under the principles of inherency, every limitation of the claim. . . .The examiner bears the burden of presenting at least a prima facie case of anticipation. Only if that burden is met, does the burden of going forward shift to the

applicant." *In re Sun*, 31 U.S.P.Q.2D (BNA) 1451 (Fed. Cir. 1993)(citations omitted)(emphasis added).

As stated by the Board of Patent Appeals and Interferences, "It is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference. *Ex parte Levy*, 17 USPQ2d 1461, 1462 (Bd. Pat. App. & Int'f 1990)(emphasis added).

Finally, as noted in § 707.06 of the Manual of Patent Examining Procedure (MPEP): "The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." (emphasis added).

It is Applicants' position that the reason for rejection of the claims set forth by the Office does not rise to the level of evidence that is required for a showing of anticipation. No individual claims are specifically called out and discussed in the rejection. The office calls out and discusses only elements or steps that were added to certain claims in the previous response. In this Office action and the previous Office action, the Office has not called out or discussed any elements or steps recited in any of the dependent claims.

It is, therefore, Applicants' position that the Office has failed to meet its burden of establishing a prima facie case of nonpatentability with respect to any of claims 1-6, 15-20, 22-26 and 28-44.

Claims rejected improperly expressed

As noted in § 707.07 of the MPEP, "A plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all claims in the group." (emphasis added).

As in the first Office action, all of the claims 1-6, 15-20, 22-26 and 28-44 were rejected in a single rejection for each of Bruce, Mitani, and Fujimoto. As such, it is Applicants' position that the bulk rejection of claims 1-6, 15-20, 22-26 and 28-44 is an improper omnibus rejection.

With the above discussion in mind, the Applicants again respectfully request that in all future Office actions relating to the present application, the Office specifically address each element of a claim individually, or at least specifically address similar claim elements from various claims as a group. Additionally, Applicants again respectfully request that the Office indicate with reasonable specificity where elements of any rejected claim are believed to be shown in an applied reference.

Request for Examiner's Affidavit

In support of the rejections of the claims, the Examiner has relied on his own personal knowledge. The Examiner has made assertions to support rejections, but has given no citation to a reference in support of those assertions. For example, the Examiner asserts the following:

> *As presently written, the claims are quite broad, to the extent that they would have been taught by a system that utilized a random access memory to store logical-to-physical address mapping information for an associated flash memory, with all the usual procedures utilized with such a map when modification or erasure has occurred.*

Applicants request that the Examiner provide a signed affidavit in support of his assertions as required by 37 CFR 1.104(d)(2).

In addition, the Examiner's statement that the "claims are quite broad" is nothing more than a personal opinion that may cast doubt on the allowability of the claims. Within regard to the language to be used in rejecting claims, Section 707.07(d) of the MPEP notes that:

> "Everything of a personal nature must be avoided. Whatever may be the examiner's view as to the utter lack of patentable merit in the disclosure of the application examined, he or she should not express in the record the opinion that the application is, or appears to be, devoid of patentable subject matter. Nor should he or she express doubts as to the allowability of allowed claims or state that every doubt has been resolved in favor of the applicant in granting him or her the claims allowed." (emphasis added.)

In future Office actions, the Applicants respectfully request that the Examiner refrain from expressing personal opinions as to the allowability of the claims.

Discussion of Claim Rejections

Claim 1 reads as follows:

1. A method comprising:

receiving a request to write data to a logical sector address of a flash memory medium;

selecting a physical sector address from a list of free physical sector addresses;

assigning the selected free physical sector address to the logical sector address forming a corresponding relationship between the addresses;

storing the corresponding relationship between the addresses in a data structure; and

writing the data into a physical sector of the flash memory medium at a location indicated by the selected free physical sector address.

Claim 1 recites selecting a free physical sector address from a list of free physical sector addresses and writing data to a physical address indicated by the selected free physical sector address. As noted on page 13, lines 11-12 of the present application, "a free physical sector is any sector that can accept data without the need to be erased first."

In all of its rejections, the Office states that "since flash memories are not radial disks, the term 'sectors' is merely a convention to describe a given amount of data." As used in the claims, sector does not merely describe a given amount of data. Rather, sector refers to a subdivision of a block of memory in flash memory. Flash memory is generally split into a number of blocks and "[e]ach block 0, 1, 2, etc. is further subdivided into K sectors 102." See Application, page 5, lines 13-14.

Furthermore, blocks and sectors in flash memory have functional differences with regard to how they are written to and erased. On page 6, lines 14-19, the present application states:

"1. Write operations to a sector can change an individual bit from a logical '1' to a logical '0', but not from a logical '0' to logical '1' (except for case No. 2 below);
2. Erasing a block sets all of the bits in the block to a logical '1';
3. It is not generally possible to erase individual sectors/bytes/bits in a block without erasing all sectors/bytes within the same block."

Therefore, the term 'sector' does not mean simply "a given amount of data" as the Office states, but has a specific meaning with regard to flash memory.

The Office asserts that Bruce's unified re-map table 20 corresponds to a list of free physical sector addresses. However, Bruce's unified re-map table 20 does not include a list of sectors (or pages) that can accept data without the need to be erased first. Bruce's unified re-map table 20 maps a requested LBA to a block. See Bruce, Fig. 5; col. 5, lines 59-65. Block counter values 46 and 48 count the number of writes to the physical flash block being accessed. See Bruce, col. 7, lines 42-45. The counter values 46 and 48 are compared to threshold values 62 and 64. When counter values 46 and 48 exceed the threshold the wear-leveling operation swaps the LBA to a different, less-used physical flash block. See Bruce, col. 7, lines 48-54.

Thus, Bruce's unified re-map table 20 keeps counts of the number of writes to a region in flash memory, and does not keep track of whether a region of flash

memory is free. In addition, Bruce's unified re-map table 20 includes a physical block address related to an LBA, and not a physical sector address.

As such, Bruce fails to teach or suggest selecting a physical sector address from a list of free physical sector addresses and writing the data into a physical sector of the flash memory medium at a location indicated by the selected free physical sector address. For at least the foregoing reasons Bruce fails to anticipate claim 1.

Regarding Mitani, the Office asserts that Mitani's RAM 4 includes a list of free physical sector addresses. Applicants have thoroughly reviewed Mitani and cannot find any teaching of a list of free physical sector addresses. Mitani stores physical addresses in task registers 40. See Mitani, col. 7, line 9. Mitani does not disclose that the physical addresses stored in the task registers 40 are physical sector addresses.

Mitani uses the word 'sector' only once. This single instance is in col. 3, line 63, reproduced here:

> "Because there are a plurality of flash memories 20a, 20b, 20c, 20d and also each of those memories may include a bad sector, internal physical addresses are not contiguous. Thus the memory card 100 is provided with the controller 1 for translating the physical addresses into logical addresses that form contiguous address space when viewed from the host end."

The foregoing passage does not indicate that the task registers 40 store physical sector addresses. Furthermore, neither the foregoing section, nor any other section of Mitani discloses free physical sector addresses.

As such, Mitani fails to teach or suggest selecting a physical sector address from a list of free physical sector addresses and writing the data into a physical sector of the flash memory medium at a location indicated by the selected free physical sector address. For at least the foregoing reasons Mitani does not anticipate claim 1.

Regarding Fujimoto, Fujimoto does not discuss a list of free physical sector addresses. Rather, Fujimoto discloses a logical block to physical block translation. At column 9, lines 54-57, Fujimoto states:

> "By employing the LTPb 152-i, the logical address (LA) can be translated into the physical address (PA) of the flash memory 15 corresponding to the logical address. This address translation is referred to as LTP (Logical Address To Physical address translation). Specifically, reference is made to the LTPb 152-i by the 14-bit logical block address (LBA) 34 in the logical address (LA), whereby, as shown in FIG. 3, the logical block address 34 is translated into the physical *block* address (PBA) 35 registered in the corresponding entry in the LTPb 152-i. Then, the least significant 14 bits (14 bits consisting of the sector address 32 and the offset 33) in the logical address are linked with the least significant bits of this physical block address 35, thereby acquiring the physical address (PA) corresponding to the logical address." (emphasis added).

The foregoing discussion makes no mention of free physical sector addresses. The least significant 14 bits of the request LBA determine the sector to which the LBA is translated. Because the sector is dependent upon the requested LBA, there is no way of knowing whether the physical address selected will correspond to a free physical address.

Applicants have reviewed the remainder of Fujimoto in detail and found nothing that teaches or suggests the concept of a list of free physical sector addresses, of selecting a physical sector address from a list of free physical sectors, or writing data into a physical sector at a location indicated by the selected free physical sector address, as recited in claim 1.

The Office states that Fujimoto mentions sectors throughout the reference. Applicants don't deny that Fujimoto mentions sectors. However, in order for Fujimoto to anticipate claim 1, Fujimoto must do more than merely discuss sectors. For anticipation, Fujimoto must discuss a list of free physical sector addresses, as well as all of the other elements in claim 1. As mentioned, Fujimoto does not discuss a number of elements recited in claim 1.

Therefore, Fujimoto fails to anticipate claim 1.

Claims 2-6 each depend in some form from claim 1 and, therefore, necessarily include all of the steps recited in claim 1. As such, each of claims 2-6 is allowable over the cited references for at least the reasons set forth with respect to claim 1. Each of claims 2-6 also specifies an additional feature or features that, together with the steps of claim 1, define a unique method that is not taught or suggested by the cited references.

Claim 15 reads as follows:

15. A computer-readable medium having computer-executable instructions for performing steps comprising:

receiving a request to write data to a logical sector address of a flash memory medium;

selecting a physical sector of the flash memory medium to store the data based on the ability of the physical sector to store the data without first being erased;

assigning a physical sector address of the selected physical sector to the logical sector address forming a corresponding relationship between the addresses;

storing the corresponding relationship between the addresses in a data structure;

writing the data into the physical sector; and

writing the logical sector address in the physical sector of the flash memory medium along with the data.

Claim 15 recites, receiving a request to write data to a logical sector address and selecting a physical sector to store the data based on the ability of the physical sector to store the data without first being erased. Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches selecting a physical sector to store the data based on the ability of the physical sector to store the data without first being erased.

Claim 15 recites assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses, and storing the corresponding relationship between the addresses in a data structure. As noted above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references. As such, the cited references do not teach either the "forming" or "storing" operations of claim 15.

Claim 15 also recites writing the logical sector address in the physical sector of the flash memory medium along with the data. Applicants could find nothing in any of the cited references that teaches writing a logical sector address in a physical sector of the flash memory medium along with the data.

In support of its rejection of claim 15, the Office states that Bruce discloses "based on the ability of the physical sector to store the data without first being erased" at column 4, lines 55 et seq. These lines are reproduced here:

> "...wear-leveling can be accomplished if both the total number of writes and the incremental number of writes to a block are stored. Dual write counters keep track of:
> 1. total number of writes to a block over its entire existence,
> 2. incremental number of writes since the block's last wear-leveling operation."

The foregoing discussion relates to wear-leveling, and specifically a way of keeping track of wear in a block of memory. Wear-leveling is scheme to detect and minimize excess writes to flash memory to provide even wear over the flash memory. See Bruce, col. 2, line 55; Abstract. Thus, the cited section above

merely discusses counting how many times a block has been written to, without regard to whether the block needs to be erased prior to storing data. As such, the cited section above does not disclose selecting a physical sector to store the data based on the ability of the physical sector to store the data without first being erased.

For at least the foregoing reasons, Bruce fails to teach or suggest the combination of steps recited in claim 15. As such, claim 15 is not anticipated by Bruce.

With regard to Mitani, the Office asserts that Mitani discloses "based on the ability of the physical sector to store the data without first being erased" at column 9, line 4, which is reproduced here:

> "After further two repetitions of steps S22, S11, S12 and S21, whether or not the task register 40a corresponding to the flash memory 20a holds a physical address is determined in step S22. The task register 40a at this time holds a physical address since no status check has not been made since the execution of step S10 as described. Thus, the judgement in step S22 results in "YES" for the first time and the process goes to step S23."

In Mitani, a status check determines whether an error occurs during writing to a physical address in flash memory. See Mitani, col. 6, lines 48-54. A physical address remains in the task register until a status check is made on the corresponding flash memory. See Mitani, col. 8, lines 1-6. Thus, the above passage merely describes a process of determining whether data was successfully

written to flash memory, and if it was not, then the data will be rewritten. See Mitani, Fig. 6, col. 9, lines 4-20.

Neither in the foregoing passage, nor anywhere else in Mitani, does Mitani mention receiving a request to write data to a logical sector address and selecting a physical sector to store the data based on the ability of the physical sector to store the data without first being erased. For at least the foregoing reasons, Mitani fails to disclose or suggest all of the elements of claim 15. Mitani, therefore, does not anticipate claim 15.

With regard to Fujimoto, the Office asserts that Fujimoto discloses "based on the ability of the physical sector to store the data without first being erased" at step S19 of Figure 6B. The textual description of step S19 is reproduced here:

> "When writing is normally performed by this re-access, a series of processes during access request acceptance is ended. In contrast, when a write error reoccurs, the block substituting process at the step S19 or later and the rewriting process targeted for the substituting block are performed."

The foregoing passage merely indicates that another block of flash memory will be substituted for a block on which a write error occurs. In addition, as discussed above, Fujimoto does not select a free physical sector address, because Fujimoto's physical sector is derived from the least significant 14 bits of the requested LBA. Therefore, Fujimoto fails to disclose selecting a physical sector to store the data based on the ability of the physical sector to store the data without first being erased.

Claims 16 – 20 each depend in some form from claim 15 and, therefore, each of these claims includes all of the steps recited in claim 15. Each of claims 16 – 20 is believed to be allowable over the cited references for at least the reasons set forth with respect to claim 15. Each of claims 16 – 20 also includes a step or steps in addition to the steps of claim 15. As such, each of claims 16 – 20 recites a unique combination of steps that is believed to be allowable over the cited references.

Claim 22 reads as follows:

22. A method comprising:

(a) receiving a request to write data to a logical sector address of a flash memory medium;

(b) assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses;

(c) storing the corresponding relationship between the addresses in a data structure;

(d) writing the data into a physical sector of the flash memory medium at a location indicated by the physical sector address;

(e) receiving a request to rewrite updated data to the logical sector address;

(f) assigning a new physical sector address to the logical sector address forming a corresponding relationship between the new physical sector address and the logical sector address;

(g) storing the corresponding relationship between the addresses from the aforementioned paragraph (f) in the data structure;

(h) writing the updated data into a physical sector of the flash memory medium at a location indicated by the new physical sector address; and

(i) marking the physical sector address from the aforementioned paragraph (b) as dirty.

Claim 22 relates to, among other things, satisfying a request to write updated data to a given logical sector address by writing the updated data to a new physical sector and assigning the physical sector address of the new physical sector to the given logical sector address.

Applicants have been unable to locate any discussion in any of the cited references related to the general concept of handling the rewriting of updated data to a logical sector address in a flash device, much less handling the rewriting of updated data in the manner recited in claim 22. With this in mind, steps (e) – (f) are clearly not taught in any of the cited references.

Claim 22 recites assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses, and storing the corresponding relationship between the addresses in a data structure. As noted

above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references. As such, the cited references do not teach either the "forming" or "storing" operations of claim 22.

Claim 22 recites marking the physical sector address from the aforementioned paragraph (b) as dirty. As noted in the present application in the last paragraph of page 14, a dirty sector is a sector that has had its data written to another physical sector. Applicants have been unable to locate any discussion in any of the cited references related to marking a physical sector address as dirty.

As described, the cited references fail to teach or suggest the combination of steps recited in claim 22. As such, claim 22 is believed to be allowable over the cited references, and such allowance is respectfully requested.

Claims 23 – 26 each depend in some form from claim 22. As such, each of claims 23-26 is necessarily allowable over the cited references for at least the reasons set forth with respect to claim 22. Each of claims 23 – 26 also includes a step or steps in addition to the steps of claim 22. As such, each of claims 23 – 26 recites a unique combination of steps that is believed to be allowable over the cited references.

Claim 28 reads as follows:

28. A system, comprising:

flash medium logic, configured to store data in a physical sector of a flash memory medium;

a table, configured to map logical sector addresses received from a file system to physical sector addresses on the flash memory medium; and

flash abstraction logic, configured to ascertain a next free physical sector on a flash memory medium and assign an address associated with the free physical sector to a logical sector address associated with a write request received from the file system.

Claim 28 recites a table that is configured to map logical sector addresses received from a file system to physical sector addresses on the flash memory medium. As previously mentioned, none of the cited references describe the use of logical-to-physical **sector** mapping.

Claim 28 also recited a flash abstraction logic that is configured to ascertain a next free physical sector on a flash memory medium and assign an address associated with the free physical sector to a logical sector address associated with a write request received from the file system. Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches ascertaining a next free physical sector to store the data based on the ability of the physical sector to store the data without first being erased.

As described, the cited references fail to teach or suggest the combination of elements recited in claim 28. As such, claim 28 is believed to be allowable over the cited references, and such allowance is respectfully requested.

Claims 29 – 35 each depend in some form from claim 28. As such, each of claims 29 - 35 is necessarily allowable over the cited references for at least the reasons set forth with respect to claim 28. Each of claims 29 - 35 also recite various features in addition to the elements of claim 28. As such, each of claims 29 - 35 recites a unique combination of elements that is believed to be allowable over the cited references.

Claim 36 reads as follows:

36. A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:

receive a request to write data to a logical sector address of a flash memory medium;

selecting a physical sector address from a list of free physical sector addresses;

assign the selected physical sector address to the logical sector address forming a corresponding relationship between the addresses;

store the corresponding relationship between the addresses in a table; and

write the data into a physical sector of the flash memory medium at a location indicated by the physical sector address.

Claim 36 recites selecting a free physical sector address from a list of free physical sector addresses and writing data to a physical address indicated by the selected free physical sector address. As noted above with respect to claim 1, Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches or suggests the concept of a list of free physical sector addresses, of selecting a physical sector address from a list of free physical sectors, or writing data into a physical sector at a location indicated by the selected free physical sector address, as recited in claim 36.

Claim 36 also recites assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses, and storing the corresponding relationship between the addresses in a data structure. As noted above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references. As such, the cited references do not teach either the "forming" or "storing" operations of claim 36.

As described, the cited references fail to teach or suggest all of the steps recited in claim 36. As such, it is believed that claim 36 is allowable over the cited references, and such allowance is respectfully requested.

Claim 37 reads as follows:

37. A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:

receive a request to write data to a logical sector address of a flash memory medium;

assign a physical sector address to the logical sector address forming a corresponding relationship between the addresses;

store the corresponding relationship between the addresses in a table;

write the data into a physical sector of the flash memory medium at a location indicated by the physical sector address;

write the logical sector address in the physical sector of the flash memory medium along with the data;

if the table is erased, then scan the flash memory medium to locate the logical sector address stored with the data;

assign the physical sector address containing the data to the logical sector address forming a reestablished corresponding relationship between the addresses; and

store the reestablished corresponding relationship between the addresses in a new table.

Claim 37 recites a computer-readable medium comprising computer-executable instructions that assign a physical sector address to a logical sector address forming a corresponding relationship between the addresses, and store the

corresponding relationship between the addresses in a table. As noted above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references. As such, the cited references do not teach either the "form" or "store" element of claim 37.

The computer executable instructions of claim 37 also write the logical sector address in the physical sector of the flash memory medium along with the data. Applicants could find nothing in any of the cited references that teaches writing a logical sector address in a physical sector of the flash memory medium along with the data.

The computer executable instructions of claim 37 also scan the flash memory medium to locate the logical sector address stored with the data if the table is erased, assign the physical sector address containing the data to the logical sector address forming a reestablished corresponding relationship between the addresses, and store the reestablished corresponding relationship between the addresses in a new table.

It follows, that since the cited references do not teach storing the correspondence between logical and physical addresses in a table, or writing a logical sector address in a physical sector of the flash memory medium along with the data, the cited references likewise do not show reestablishing a new table if old table is erased, as recited in the last three elements of claim 37.

As described, the cited references fail to teach or suggest all of the steps recited in claim 37. As such, it is believed that claim 37 is allowable over the cited references, and such allowance is respectfully requested.

Claim 38 reads as follows:

38. A system for tracking sectors in a flash memory medium, comprising:

means for receiving a request to retrieve data stored in the flash memory medium from a location indicated by a logical sector address;

means for locating a physical sector address corresponding to the specific logical sector address in a table; and

means for reading the data stored in the flash memory medium from the physical sector address located from the table.

Claim 38 recites means for locating a physical sector address corresponding to the specific logical sector address in a table. As previously mentioned, none of the cited references describe the use of logical-to-physical **sector** mapping. More particularly, the cited references do not show locating a physical **sector** address corresponding to the specific logical **sector** address in a table.

As described, the cited references fail to teach or suggest all of the steps recited in claim 38. As such, it is believed that claim 38 is allowable over the cited references, and such allowance is respectfully requested.

Claims 39 – 44 each depend in some form from claim 38. As such, each of claims 39 - 44 is necessarily allowable over the cited references for at least the reasons set forth with respect to claim 38. Each of claims 39 - 44 also recite various features in addition to the elements of claim 38. As such, each of claims 39 - 44 recites a unique combination of elements that is believed to be allowable over the cited references.

Conclusion

Claims 1 – 6, 15 – 20, 22 – 26, and 28 - 44 are believed to be in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Office is encouraged to contact the undersigned attorney to discuss the unresolved issue.

Respectfully Submitted,

Dated: 9/20/04 By: Damon A. Rieth

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